What is claimed is:

1. A one-time programmable memory device, comprising:
an isolation layer for defining an active area of a substrate;
an oxide layer formed on the active area;
a floating gate formed over the active area and the isolation layer;
an inter-gate dielectric layer formed on the floating gate; and
a control gate formed on the inter-gate dielectric layer.

2. The one-time programmable memory device of claim 1, further comprising a source region and a drain region formed in the active area at least one of under and adjacent both sides of the control gate.

3. The one-time programmable memory device of claim 1, wherein a portion of the floating gate formed over the active area is narrower than a portion of the floating gate formed over the isolation layer.

4. The one-time programmable memory device of claim 1, wherein the control gate is formed over the floating gate.

5. The one-time programmable memory device of claim 1, wherein the control gate is formed so as to enclose at least one sidewall of the floating gate.

6. The one-time programmable memory device of claim 1, wherein the inter-gate dielectric layer includes a silicon nitride layer.

7. The one-time programmable memory device of claim 6, wherein the inter-gate dielectric layer includes a composite layer having a silicon oxide layer and a silicon nitride layer.

8. The one-time programmable memory device of claim 6, wherein the inter-gate dielectric layer includes a composite layer having a silicon oxide layer, a silicon nitride layer, and a silicon oxide layer.

9. An integrated circuit, comprising:

a memory device including an isolation layer for defining an active area of a substrate, a tunnel oxide layer formed on the active area, a floating gate formed over the active area and the isolation layer, an inter-gate dielectric layer formed on the floating gate, and a control gate formed on the inter-gate dielectric layer;

a first transistor including a first gate, a first gate oxide layer interposed between the first gate and the substrate, and a first source region and a first drain region formed in the active area at least one of under and adjacent both sides of the first gate; and

a second transistor including a second gate, a second gate oxide layer interposed between the second gate and the substrate, and a second source region and a second drain region formed in the active area at least one of under and adjacent both sides of the second gate.

10. The integrated circuit of claim 9, wherein the memory device further includes a source region and a drain region formed in the active area at least one of under and adjacent both sides of the control gate.

11. The integrated circuit of claim 9, wherein the second gate oxide layer is thinner than the first gate oxide layer.

12. The integrated circuit of claim 9, wherein the second gate oxide layer is thinner than the tunnel oxide layer, and the first gate oxide layer is thicker than the tunnel oxide layer and the second gate oxide layer.

13. The integrated circuit of claim 12, wherein the first gate and the second gate are formed of the same material as the control gate.

14. The integrated circuit of claim 9, wherein the second gate oxide layer has the same thickness as the tunnel oxide layer, and the first gate oxide layer is thicker than the tunnel oxide layer and the second gate oxide layer.

15. The integrated circuit of claim 14, wherein the first gate and the second gate are formed of the same material as the control gate.

16. An integrated circuit, comprising:

a plurality of isolation layers for defining a first area, a second area, and a third area in a substrate;

a memory device including a floating gate formed over the first area and at least one isolation layer of the plurality of isolation layers, an inter-gate dielectric layer formed on the floating gate and including a composite layer having a silicon oxide layer and a silicon nitride layer, and a control gate formed on the inter-gate dielectric layer;

a first transistor including a first gate formed of the same material as the control gate, wherein the first gate is formed in the second area of the substrate on a first gate oxide layer having a thickness greater than or equal to a thickness of a tunnel oxide layer formed on the substrate, and a first source region and a first drain region formed in the second area at least one of under and adjacent both sides of the first gate; and

a second transistor including a second gate formed of the same material as the control gate, wherein the second gate is formed in the third area of the substrate on a second gate oxide layer thinner than the first gate oxide layer, and a second source region and a second drain region formed in the third area at least one of under and adjacent both sides of the second gate.

17. The integrated circuit of claim 16, wherein a portion of the floating gate over the first area is narrower than a portion of the floating gate over the at least one isolation layer.

18. A method of fabricating an integrated circuit, comprising:

forming a plurality of isolation layers for defining a first active area and a second active area in a substrate;

forming a tunnel oxide layer on the substrate;

forming and patterning a floating gate material on a surface of the substrate including the tunnel oxide layer, to form a floating gate;

forming an inter-gate dielectric layer including a composite layer having a silicon oxide layer and a silicon nitride layer on a surface of the substrate including the floating gate;

etching a portion of the inter-gate dielectric layer in the second active area to form a first gate oxide layer of a high voltage transistor, the first gate oxide layer being thicker than the tunnel oxide layer;

forming and patterning a conductive material on a surface of the substrate including the inter-gate dielectric layer and the first gate oxide layer, to form a control gate and a first gate of the high voltage transistor;

forming an interlayer insulating layer comprising a contact hole on a resultant structure; and

forming a metal interconnection connectable to the control gate via the contact hole.

19. The method of claim 18, wherein the substrate includes a third active area, and further comprising:

etching a portion of the inter-gate dielectric layer in the third active area;

forming a second gate oxide layer of a low voltage transistor, the second gate oxide layer having a thickness less than or equal to a thickness of the tunnel oxide layer; and

forming a second gate of the low voltage transistor in the third active area when forming and patterning the conductive material to form the control gate and the first gate of the high voltage transistor.

20. The method of claim 18, further comprising forming a source region and a drain region in each of the first active area and the second active area.

21. The method of claim 19, further comprising forming a source region and a drain region in each of the first active area, the second active area, and the third active area.

22. The method of claim 18, further comprising implanting ions into the first active area of the substrate to adjust a threshold voltage.

23. The method of claim 18, wherein at least one of the floating gate and the control gate is formed of a material selected from the group consisting of a noble

metal, a noble metal oxide, a conductive oxide, and a combination of the noble metal, the noble metal oxide, and the conductive oxide.

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